TITLE	DOC No. RFD-20220826006-003	
400G QSFP-DD DR4 500m Transceiver	REVISION : 01	AUTHORIZED BY : Albert Lin
	DATE : 2026.02.06	CLASSIFICATION : Optical Transceiver

1. General Description

The Transceiver is a high-performance, cost-effective module for optical data communication applications supporting 400G Ethernet. The Transceiver is designed to operate in switch and router applications supporting QSFP-DD MSA / 400G DR4 compliant traffic for up to 500m links. The Transceiver can convert 8-channel 53.125Gb/s electrical data to 4-channel 106.25Gb/s optical signals. Similarly, it optically converts 4-channel 106.25Gb/s optical signals to 8-channel electrical data output on the receiver side. It has been designed to withstand the maximum range of external operating conditions including temperature, humidity and EMI. The module offers very high functionality and feature integration, accessible via a two-wire serial interface.

2. Production Features

- QSFP-DD MSA compliant
- 8x53.125Gb/s PAM4 electrical interface (400GAUI-8)
- Maximum power consumption 8W
- MPO-12 APC connector
- Up to 500m transmission on single mode fiber
- Operating case temperature: 0℃~70℃
- Single 3.3V power supply
- RoHS-6 compliant

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3. Production Application

- 400GBASE-DR4 Ethernet
- QSFP-DD MSA Rev 5.1
- CMIS Rev 4.0
- GR-468-CORE

4. Production Description

3.1 Product Name and Series Numbers

400G QSFP-DD DR4 Transceiver

JPC P/N	Wavelength (nm)	Distance	Power (dBm)	Sen. (dBm)	Connector	Temp.
P68***GRCB*5-* P68610GRCBB5-M	1310nm	500m	-5.9~4	-4.4	MPO-SMF	C

Note-1：* Indicates the customer code.**

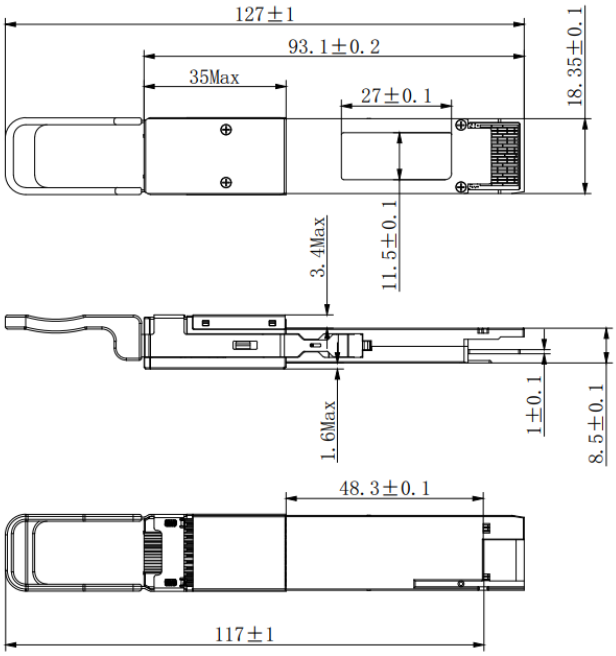
Note-2：* Indicates the Solution code.

Note-3：* Indicates the Compatible code.

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3.2 Dimension, Materials, Plating and Marking



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5. Product Specification

Absolute Maximum Ratings

Parameters	Symbol	Min	Max	Units
Case Operating Temperature	T_{OP}	0	70	°C
Power Supply Voltage	*Vcc*	-0.5	3.6	V
Storage Temperature Range	T_{ST}	-40	85	°C
Operating Relative Humidity	*RH*	5	85	%
Damage Threshold, each lane		5		dBm

Recommended Operating Conditions

Parameters	Symbol	Min	Max	Units
Case temperature	Tcase	0	70	℃
Supply Voltage	VCC	3.135	3.465	V
Supply Current	ICC		2552	mA
Module Power Dissipation	P		8	W

Transmitter Characteristics, Optical / Eletrical

Parameters	Symbol	Min	Typical	Max	Units
Signaling Speed per Lane		53.125±100			GBd
Modulation format		PAM4			
Lane wavelength(range)		1304.5	1311	1317.5	
Side-mode suppression Ratio	SMSR	30			dB
Average launch power, eachlane	TXPx	-2.9		4	dBm
Outer Optical ModulationAmplitude per Lane	OMAouter	-0.8		4.2	dBm

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Launch power in OMAouter minus TDECQ, each lane		-2.2			dBm
Transmitter and dispersionpenalty eye closure for PAM4, each lane	TDECQ			3.4	dB
Average Launch Power of OffTransmitter, each lane				-15	dBm
Optical Extinction Ratio	ER	3.5			dB
RIN17.1OMA				-136	dB/Hz
Optical return loss tolerance				21.4	dB
Transmitter reflectance				-26	dB
Differential pk-pk input Voltage tolerance	Vpp	26.5625±100ppm			GBd
Differential pk-pk input Voltage tolerance	Vpp		900		mV
DC Common Mode Voltage	Vcm	-350		2850	mV
Differential Termination Resistance Mismatch		-10		10	%
Differential Input Return Loss		IEEE 802.3-2018 Equation (83E-5)			dB
Differential to Common Mode Input Return Loss		IEEE 802.3-2018 Equation (83E-6)			dB
Module Stressed Input Test		IEEE 802.3bs 120E.3.4.1			

Receiver Optical Characteristics

Parameters	Symbol	Min	Typical	Max	Units
Signaling Speed per Lane		53.125±100			GBd
Modulation format		PAM4			
Lane wavelength(range)		1304.5	1311	1317.5	
Average receive power,per lane	RXPx	-5.9		4	dBm
Receive power OMA outer perlane	OMA outer			4.2	dBm
Receiver reflectance	Rfl			-26	dB

JPC connectivity

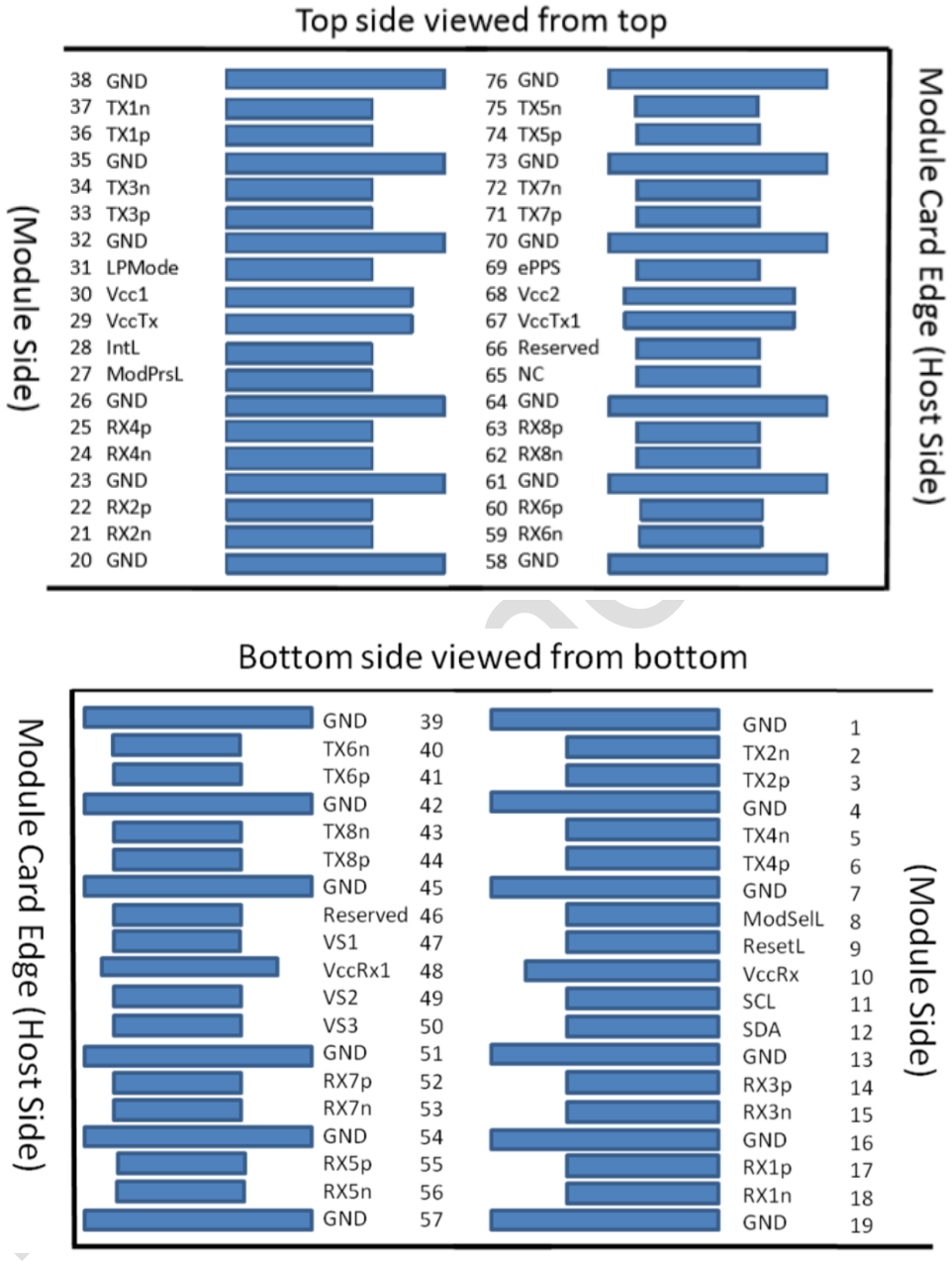
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Receiver sensitivity (OMAouter), each lane				-4.4	dBm
Stressed Sensitivity (OccMAouter) per lane	S			-1.9	dBm
Losa		-15			dBm
Losd				-8.4	dBm
Losh		0.5			dB
Electrical Data Rate, each lane		26.5625±100ppm			GBd
Differential Termination Resistance Mismatch		-10		10	%
Differential output Voltage pk-pk	Vpp			900	mV
DC Common Mode Voltage	Vcm	-350		2850	mV
Differential output return loss		IEEE 802.3-2018 Equation (83E-2)			dB
Common to differential mode conversion return loss		IEEE 802.3-2018 Equation (83E-3)			dB

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5.Pin Assignments



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Electrical Pin Definition

Host PCB	Logic	Symbol	Description	Notes
1		GND	Ground	Note1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	
4		GND	Ground	Note1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	
7		GND	Ground	Note1
8	LVTTL-I	ModSelL	Module Select	
9	LVTTL-I	ResetL	Module Reset	
10		Vcc Rx	+3.3V Power Supply Receiver	Note2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	
12	LVCMOS-I/O	SDA	2-wire serial interface data	
13		GND	Ground	Note1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	
15	CML-O	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	Note1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	
18	CML-O	Rx1n	Receiver Inverted Data Output	
19		GND	Ground	Note1
20		GND	Ground	Note1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	Note1

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24	CML-O	Rx4n	Receiver Non-Inverted Data Output	
25	CML-O	Rx4p	Receiver Inverted Data Output	
26		GND	Ground	Note1
27	LVTTL-I	ModPrsL	Module Present	
28	LVTTL-I	IntL	Interrupt	
29		VccTx	+3.3V Power supply transmitter	Note2
30		Vcc1	+3.3V Power supply	Note2
31	LVTTL-I	LPMode	Low Power Mode	
32		GND	Ground	Note1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	
34	CML-I	Tx3n	Transmitter Inverted Data Input	
35		GND	Ground	Note1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	
37	CML-I	Tx1n	Transmitter Inverted Data Input	
38		GND	Ground	Note1
39		GND	Ground	Note1
40	CML-I	Tx6n	Transmitter Inverted Data Input	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	
42		GND	Ground	Note1
43	CML-I	Tx8n	Transmitter Inverted Data Input	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	
45		GND	Ground	Note1
46		Reserved	For future use	Note3
47		VS1	Module Vendor Specific 1	Note3
48		VccRx1	+3.3V Power supply	Note2

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49		VS2	Module Vendor Specific 2	Note3
50		VS3	Module Vendor Specific 3	Note3
51		GND	Ground	Note1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	
53	CML-O	Rx7n	Receiver Inverted Data Output	
54		GND	Ground	Note1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	
56	CML-O	Rx5n	Receiver Inverted Data Output	
57		GND	Ground	Note1
58		GND	Ground	Note1
59	CML-O	Rx6n	Receiver Non-Inverted Data Output	
60	CML-O	Rx6p	Receiver Inverted Data Output	
61		GND	Ground	Note1
62	CML-O	Rx8n	Receiver Non-Inverted Data Output	
63	CML-O	Rx8p	Receiver Inverted Data Output	
64		GND	Ground	Note1
65		NC	No Connect	Note3
66		Reserved	For Future Use	Note3
67		VccTx1	+3.3V Power supply	Note2
68		Vcc2	+3.3V Power supply	Note2
69	LVTTL-I	ePPS	Precision Time Protocol (PTP) reference clock input	Note3
70		GND	Ground	Note1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	
72	CML-I	Tx7n	Transmitter Inverted Data Input	
73		GND	Ground	Note1

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74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	
75	CML-I	Tx5n	Transmitter Inverted Data Input	
76		GND	Ground	Note1

Notes:

1. *QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.*
2. *VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 6 from QSFP-DD MSA. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.*
3. *All Vendor Specific, Reserved and No Connect and ePPS(if not used) pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF.*
4. *Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A,2A,3A,1B,2B,3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A,1B will then occur simultaneously, followed by 2A,2B, followed by 3A,3B.*

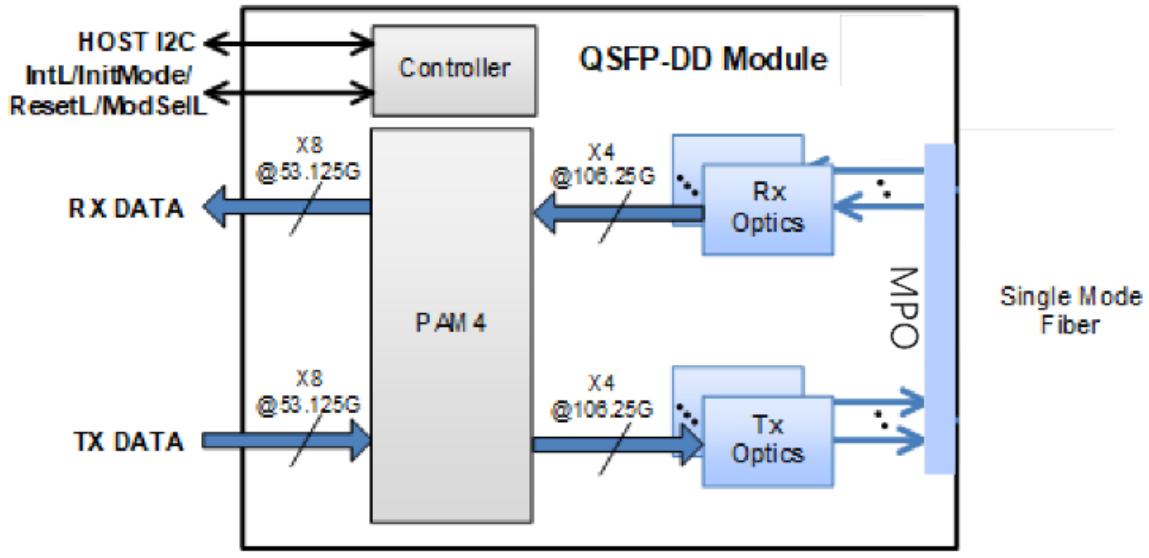
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Digital Diagnostic Specification

Parameter	Symbol	Min	Typical	Max	Units	Notes
Transceiver Case Temperature	DMI_Temp	-3		+3	℃	Over operating temp
Supply voltage monitor absolute error	DMI _VCC	-3%		+3%	V	Full operating range
Channel RX power monitor absolute error	DMI_RX	-3		+3	dB	Per channel
Channel Bias current monitor	DMI_Ibias	-10%		+10%	mA	Per channel
Channel TX power monitor absolute error	DMI_TX	-3		+3	dB	Per channel

Block Diagram of Transceiver

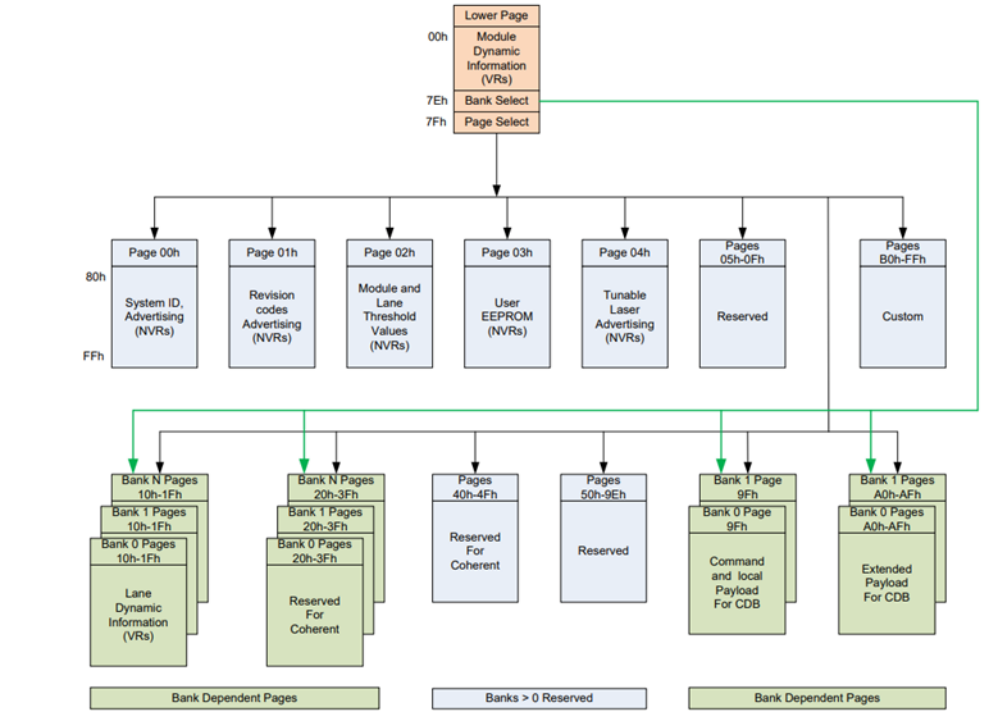


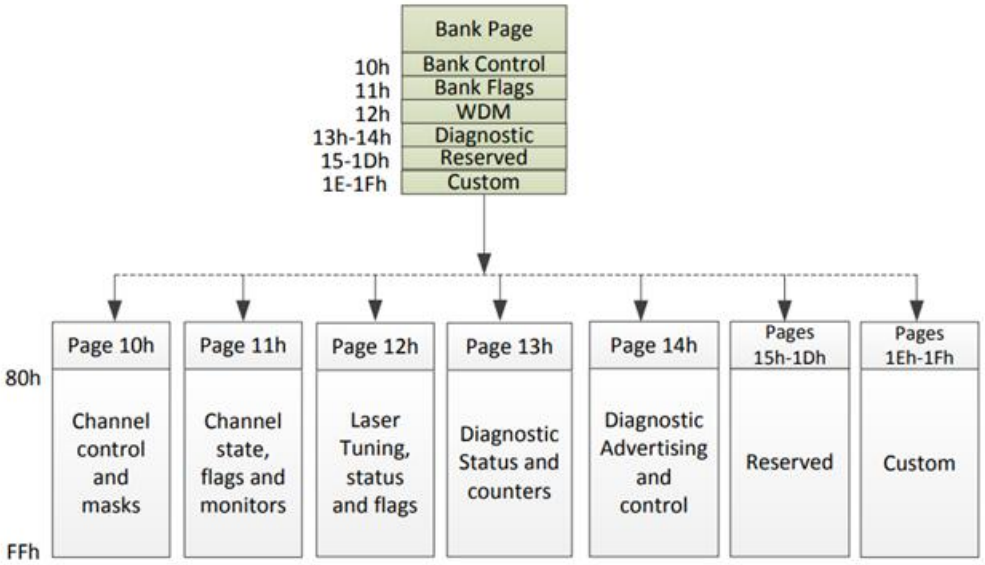
<Transmitter Section>: The MQD-35F2C converts 8-channel 53.125Gb/s electrical data to 4-channel 1310nm 106.25Gb/s optical signals for 425Gb/s optical transmission.

<Receiver Section>: Similarly, it optically converts 4-channel 1310nm 106.25Gb/s optical signals to 8-channel electrical data output on the receiver side.

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Memory map





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6.Modification History

Rev.	Comments	Date	Originator	Approval
01	Preliminary Draft	2026.02.06	Albert Lin	Mike Sun

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